L Number	Hits	Search Text	DB	Time stamp
1	81653	(via hole opening) same (interconnect interconnection)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 16:32
2	26548	((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 16:34
3	94	(((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))) same ((roll and column) (parallel and perpendicular))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:17
4	7404	(((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))) same metal	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 16:55
5	46	((((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))) same metal) same (width and length)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 16:56
6	46	(((((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))) same metal) same (width and length)) not ((((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))) same ((roll and column) (parallel and perpendicular)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:12
7	174704	257/$7.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:12
8	135921	438/$7.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:13
9	95871	361/$7.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:13
10	166400	29/$7.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:14
11	517917	257/$7.ccls. 438/$7.ccls. 361/$7.ccls. 29/$7.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:14
12	10863	(((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))) and (257/$7.ccls. 438/$7.ccls. 361/$7.ccls. 29/$7.ccls.)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:14

13	10371	((((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))) and (257/$7.ccls. 438/$7.ccls. 361/$7.ccls. 29/$7.ccls.)) and (metal metallization line)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:16
14	7306	((((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))) and (257/$7.ccls. 438/$7.ccls. 361/$7.ccls. 29/$7.ccls.)) and (metal metallization line)) and (dielectric insulation)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:16
15	5065	((((((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))) and (257/$7.ccls. 438/$7.ccls. 361/$7.ccls. 29/$7.ccls.)) and (metal metallization line)) and (dielectric insulation)) and ((roll and column) (parallel and perpendicular) (width and length) (top and (side bottom)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:20
16	3702	(((((((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))) and (257/$7.ccls. 438/$7.ccls. 361/$7.ccls. 29/$7.ccls.)) and (metal metallization line)) and (dielectric insulation)) and ((roll and column) (parallel and perpendicular) (width and length) (top and (side bottom)))) and (spacing spaced space direction)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:35
17	53	(((((((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))) and (257/$7.ccls. 438/$7.ccls. 361/$7.ccls. 29/$7.ccls.)) and (metal metallization line)) and (dielectric insulation)) and ((roll and column) (parallel and perpendicular) (width and length) (top and (side bottom)))) and (spacing spaced space direction)) and equidistant	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:22
18	2089	(((((((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))) and (257/$7.ccls. 438/$7.ccls. 361/$7.ccls. 29/$7.ccls.)) and (metal metallization line)) and (dielectric insulation)) and ((roll and column) (parallel and perpendicular) (width and length) (top and (side bottom)))) and (spacing spaced space direction)) and wafer	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:43
20	1833	(((((((((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))) and (257/$7.ccls. 438/$7.ccls. 361/$7.ccls. 29/$7.ccls.)) and (metal metallization line)) and (dielectric insulation)) and ((roll and column) (parallel and perpendicular) (width and length) (top and (side bottom)))) and (spacing spaced space direction)) and (semiconductor chip die wafer)) and (driving force localized stress gradient stress)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:46

19	3581	(((((((integrated adj circuit) ic device) same ((via hole opening) same (interconnect interconnection))) and (257/$7.ccls. 438/$7.ccls. 361/$7.ccls. 29/$7.ccls.)) and (metal metallization line)) and (dielectric insulation)) and ((roll and column) (parallel and perpendicular) (width and length) (top and (side bottom)))) and (spacing spaced space direction)) and (semiconductor chip die wafer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/22 17:47

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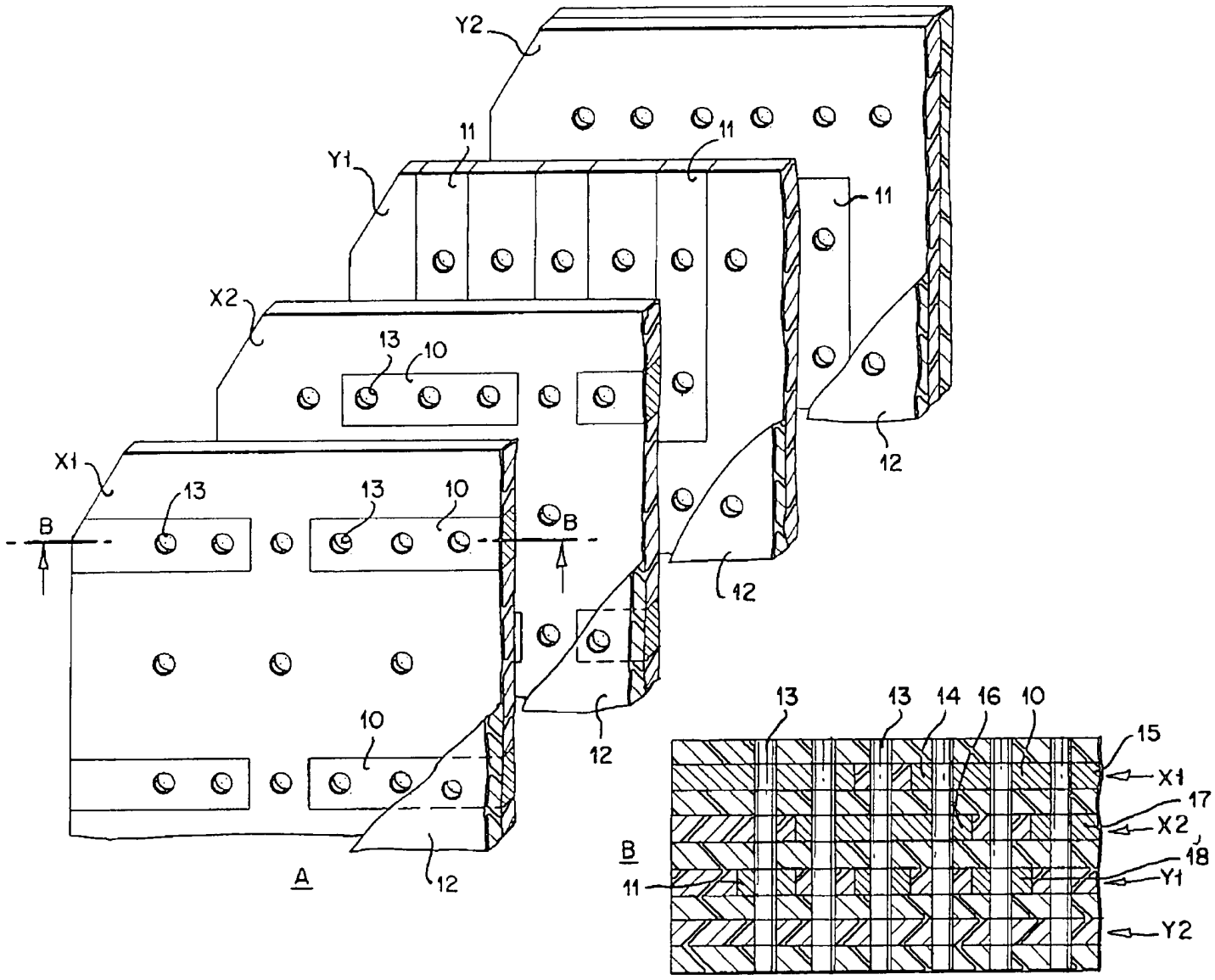
2p. A simulator board structure is for determining the feasibility in design of conductive interconnector paths in semiconductor integrated circuits utilizing such interconnectors. In automated fabrication of integrated circuits, one approach is to utilize a master semiconductor chip having a standardized array of active and passive elements. A desired circuit is tailored by selectively forming interconnections between combinations of these active and passive elements. Of necessity, in such a structure, the interconnectors have to cross over each other. Such crossovers are accomplished by a multilayer interconnector structure. - This simulator is capable of simulating the selected interconnector pattern from information stored in a conventional punched card. The simulator comprises a plurality of planes, each of which contains discrete insulated strips of conductive material. The planes are separated from each other by insulative layers. The structure shown contains four such planes X1 and X2 in which the conductive strips 10 are disposed parallel to the X axis and planes Y1 and Y2 in which the conductive strips 11 are disposed parallel to the Y axis. Insulating layers 12 separate the four planes. Openings 13 extend through the entire composite and are disposed so that, with the exception of the peripheral conductive strips, substantially all of conductive strips 10 and 11 have three apertures 13 passing through. - The strips are disposed so that the apertures passing through the ends of the strips are in registration with apertures passing through the ends of parallel strips in the next level. The apertures passing through the center of each conductive strip are in registration with apertures passing through the center of conductive strips disposed in a direction perpendicular to such strips on different levels. In drawing B, the apertures passing through ends 14 and 15 in the conductive strips on the X1 level are in registration with apertures

passing through ends 16 and 17 in conductive strips on the X2 level. The aperture passing through the center of the same conductive strip on the X1 level is in registration with the aperture passing through the center of strip 18 on the Y1 level. In forming the conductive path by inserting a combination of pins passing through either the end or the center aperture in given conductive strips, the conductive paths are formed involving the connective strips on all four levels. - The computer which controls the eventual formation of interconnections on the final can may be so programmed that the punch card storing information relative to the arrangement of the chip connector pattern contains a combination of apertures coinciding with the apertures to be interconnected on the simulator. Thus, the punch card can be placed over the simulator and pins inserted through the apertures in the card to form the pattern on the simulator. The simulator can then be tested to determine the accuracy of the pattern. If the pattern is accurate, the card can then be used in the fabrication of the chips.


Y2
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